

# ① JFET (Part 1)

→ FET is field effect transistor

→ FET is unipolar, the current flow between 2 terminals (Source & Drain) is controlled by electric field applied to the third terminal (gate)

∴ Current is conducted only by majority charge carriers  $\begin{matrix} \nearrow \text{holes} \\ \searrow \text{electrons} \end{matrix}$

## Advantages & disadvantages of JFET

Adv.

① FET is VCCS (Voltage Controlled Current Source), while BJT is (CCCS) current controlled current source

② FET has large input impedance, so it is preferred than BJT as I/P stage to multistage amplifier

③ FET generates lower noise level than BJT.

④ FET is more temperature stable than BJT.

⑤ FET is easier to be fabricated than BJT.

⑥ FET act as VCR (Voltage Controlled Resistor).

DisAdv

1- FET has poor frequency response (Low BW)

2- Poor linearity (non linear relation between  $I_D, V_{GS}$ )

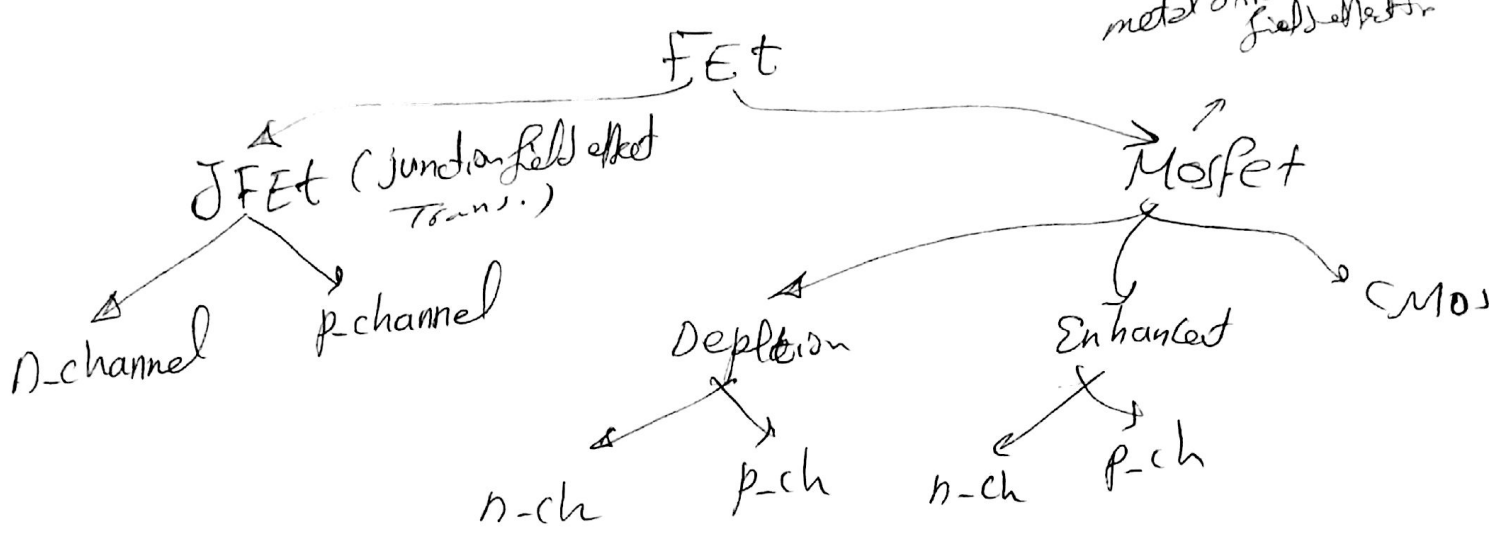
3. Due to static charges → Damage occurred.

## FET Uses

Camera, Laptop, USB drive, Flash memory, CPU, --- etc.

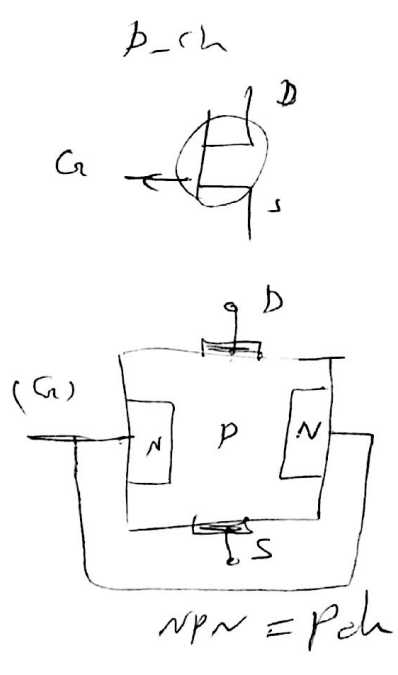
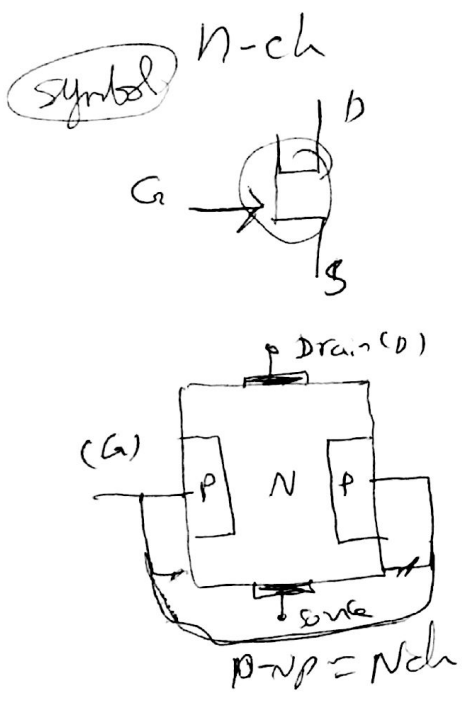
(2)

metal oxide semi-conductor field effect tr.



① JFET  $\left\{ \begin{array}{l} n\text{-ch} \rightarrow npn \\ p\text{-ch} \rightarrow pnp \end{array} \right.$

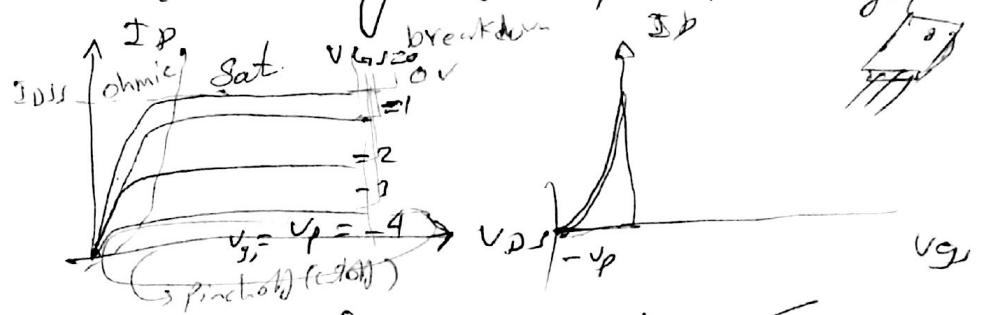
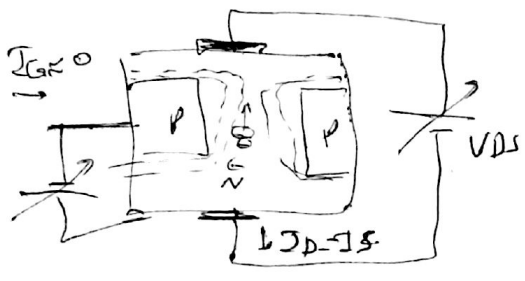
3 terminal device



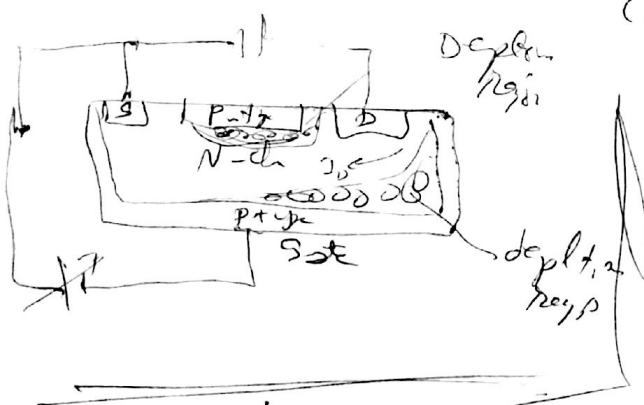
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- The N-channel consists of N-type semiconductor & P-type on both side.
- the channel is resistive path,  $V_{DS}$  drive a current  $I_D$
- JFET has P-N junction (gate-to-channel) junction. & it is always be (Reverse biased) in most applications, and hence only very small leakage current will flow in gate terminal  $\Rightarrow$  Causing large input impedance.



(N) channel  $V_{GS} < 0$



① At  $V_{GS} = 0$   
 \* as  $V_{DS}$  increase, channel resistance (increase), because increase of channel depletion region

At  $V_{GS} = 0$ ,  $V_{DS} = -V_p$  is called pinch-off voltage. In this region, the channel is narrowed at the drain end. The current  $I_D$  is constant and equal to  $I_{DSS}$ .  
 In case of pinch off  $\rightarrow V_{DS} = -V_p, V_{GS} = 0, I_D = I_{DSS}$

As  $V_{GS}$  becomes more negative, the depletion regions expand further into the channel, reducing the width of the channel and thus the current  $I_D$ .  
 The relationship between  $I_D$  and  $V_{GS}$  is given by the equation:  $I_D = I_{DSS} (1 - V_{GS}/V_p)^2$

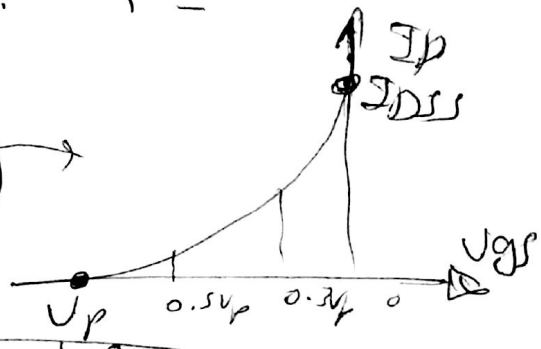
2- Increasing  $V_{GS}$  in (-ve) direction

channel depletion region (channel is completely depleted) of charge carriers (Pinch-off)

at  $V_{GS} = -V_p$  |  $I_D = 0$  ,  $V_{DS}$  is small

(shockley eq<sup>n</sup>)  $V_{GS}$  &  $I_D$  relation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$



note  $I_G = 0$  ,  $I_S = I_D$

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### Biasing of JFET

fixed bias

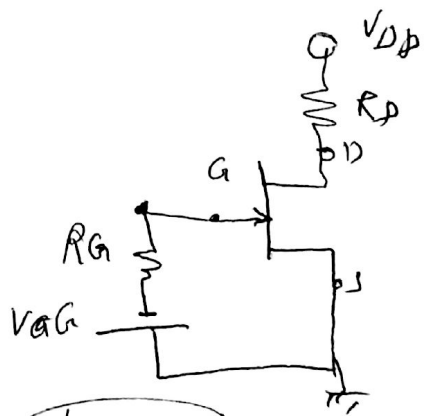
self bias

voltage divider Bias

#### 1) Fixed Bias

$I_G = 0$   
 $-V_{GG} - V_{GS} = I_G R_G$   
 $\therefore V_{GS} = -V_{GG}$

$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$   
 $V_{DS} = V_{DD} - I_D R_D$



$V_S = 0$  ,  $V_D = V_{DS}$   
 $V_G = V_{GS}$

JFET, Fixed Bias.

EX(1)  $I_{DSS} = 10\text{mA}$ ,  $V_p = -8\text{V}$ ,  $R_G = 1\text{M}\Omega$   
 $R_D = 2\text{k}\Omega$ ,  $V_{DD} = 20\text{V}$ ,  $V_{GG} = 2\text{V}$ ,  $V_{GS} =$

Find  $V_{GSQ}$ ,  $I_{DQ}$ ,  $V_{DSQ}$ ,  $V_D$ ,  $V_S$  &  $V_G$

Sol

$$V_{GS} = -V_{GG} = -2\text{V}$$

$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10 \times 10^{-3} \left(1 - \frac{-2}{-8}\right)^2 = 5.625\text{mA}$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D = 20 - 5.625 \times 10^{-3} \times 2 \times 10^3 = 8.75\text{V}$$

$$V_D = V_{DS} = 8.75$$

$$V_S = 0$$

$$V_G = V_{GSQ} = -2\text{V}$$

(التيار الذاتي للتيار)

(Self Biasing)

$$V_G = 0$$

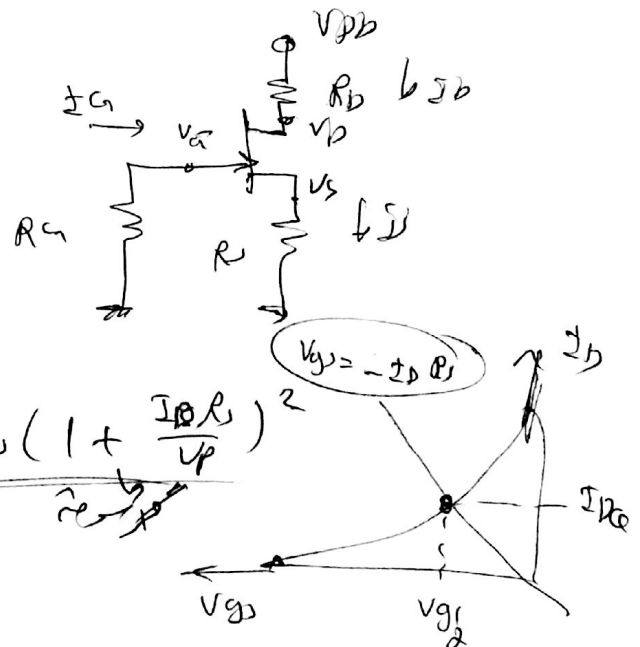
$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S = 0 - I_D R_S$$

$$V_{GS} = -I_D R_S \rightarrow \sqrt{\quad}$$

$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2 = \frac{I_{DSS} \left(1 + \frac{I_{DQ} R_S}{V_p}\right)^2}{\quad}$$

كل الركنين في  $I_D$   $V_{GS}$



$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$